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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,739	11/09/2005	Yasuhiro Okamoto	029437-0108	7288
22428 7590 03/04/2009 FOLEY AND LARDNER LLP SUITE 500 3000 K STREET NW WASHINGTON, DC 20007				
EXAMINER SALERNO, SARAH KATE				
ART UNIT 2814		PAPER NUMBER		
MAIL DATE 03/04/2009		DELIVERY MODE PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/538,739

Applicant(s)

OKAMOTO ET AL.

Examiner

SARAH K. SALERNO

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SG/US)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/12/09 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6 and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Martinez et al. (US PGPub 2003/0235974).

Claim 1: Martinez teaches A field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer and an electron supply layer [0038], a source electrode (65/66) and a drain electrode 65/66) formed on the semiconductor layer structure while being separated from each other, a

gate electrode (74) arranged between said source electrode and said drain electrode, and an insulating film (71,72,73) formed on said Group III nitride semiconductor layer [0030], wherein, said gate electrode has a field plate portion (75) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said insulating film is a multilayered film including a first insulating film (71,72) and a second insulating film (73), said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film (FIG. 8; [0030, 0034-0048]).

Claim 2: Martinez teaches the second insulating film is laminated on said first insulating film (FIG. 8).

Claim 3: Martinez teaches the thickness of said first insulating film is not more than 150 nm (FIG. 8).

Claim 4: Martinez teaches a dielectric constant of said second insulating film (38) is not more than 3.5 (FIG. 3).

Claim 5: Martinez teaches said insulating film including said multilayered film is formed while being separated from said gate electrode, and said second insulating film is provided between said first insulating film and said gate electrode (FIG. 8).

Claim 6: Martinez teaches said second insulating film is provided between said first insulating film and said gate electrode and said second insulating film is positioned below said field plate portion, and said multilayered film including said first insulating

film and said second insulating film is positioned between a drain-side end portion of said field plate portion and said drain electrode (FIG. 8).

Claim 8: Martinez teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer and an electron supply layer, a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode (16) arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said insulating film (71,72,73) is made of a compound containing silicon, nitrogen and oxygen as constituent elements (FIG. 8; [0030, 0034-0048]).

Claim 9: Martinez teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by channel layer and an electron supply layer, a source electrode (39/40) and a drain electrode (39/40) formed on the semiconductor layer structure while being separated from each other, a gate electrode (42) arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion formed on said insulating film (35) while said field plate portion has a visored shape that overhangs a gate side of said insulating

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film between said gate electrode and said drain electrode, and said insulating film has dielectric constants not more than 3.5 (FIG. 3; [0015-0026, 0030]).

Claim 10: Martinez teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer and an electron supply layer, a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said gate electrode side of said insulating film between said gate electrode and said drain electrode is made of an insulating material having dielectric constants not more than 4, and said drain electrode side of said insulating film is made f an insulating material containing silicon and nitrogen as constituent elements (FIG. 3; [0015-0026, 0030]).

Claim 11: Martinez teaches the drain electrode side of said insulating film is made of an insulating material containing silicon, nitrogen, and oxygen as the constituent elements.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (JP 09-307097) in view of Martinez et al. (US PGPub 2003/0235974), as applied to claim 1 above, and further in view of Parikh et al. (US PGPub 2003/0020092).

Regarding claim 7, as described above, Martinez substantially reads on the invention as claimed, except Martinez does not teach a third insulating film on said second insulating film, the third insulating film being made of a compound containing silicon and nitrogen as the constituent elements. Parikh teaches adding an additional dielectric layer of SiN on the surface of the existing insulating layers to further protect the device from passivation and impurities that can damage the device during handling [0038]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Martinez to include a third dielectric layer of SiN to further protect the device from passivation and impurities that can damage the device during handling as taught by Parikh [0038].

6. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martinez et al. (US PGPub 2003/0235974), in view of Inoue et al. (US PGPub 2001/0015446 of record).

Regarding claim 14, as described above, Martinez substantially reads on the invention as claimed, except Martinez does not teach the semiconductor layer structure includes said channel layer made of $\text{In}_x\text{Ga}_{1-x}\text{N}$ ($0 \leq x \leq 1$) and said electron supply layer made of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ ($0 < y \leq 1$). Inoue teaches teach the semiconductor layer structure

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includes a channel layer made of $\text{In}_x\text{Ga}_{1-x}\text{N}$ ($0 \leq x \leq 1$) and an electron supply layer made of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ ($0 < y \leq 1$) to reduce leakage current and/or improve voltage breakdown level (abs, [0029], clm. 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Martinez to have included the channel and electron supply layer required by the claim to reduce leakage current and/or improve voltage breakdown level as taught by Inoue.

Claim 18: Inoue teaches a semiconductor layer structure has a structure in which the channel layer made of $\text{In}_x\text{Ga}_{1-x}\text{N}$ ($0 \leq x \leq 1$), the electron supply layer made of $\text{Al}_y\text{Ga}_{1-y}\text{N}$ ($0 < y \leq 1$), and a cap layer made of GaN are sequentially laminate [0050]. Inoue does teach these layers are sequentially laminate, however, it is noted that "The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martinez et al. (US PGPub 2003/0235974) as applied to claim 1 above, and further in view of Mizuta et al. (US Patent 6,483,135 of record).

Regarding claim 15, as described above, Martinez substantially reads on the invention as claimed, except Martinez does not teach the contact layers are arranged between said source electrode and a surface of said semiconductor layer structure and

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between said drain electrode and a surface of said semiconductor layer structure, respectively. Mizuta teaches the contact layers (3) are arranged between said source electrode (7/8) and a surface of said semiconductor layer (2) structure and between said drain electrode (7/8) and a surface of said semiconductor layer structure, respectively to improve device performance (FIG. 7; Col. 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Martinez to have the contact layers between the source/drain electrodes and the semiconductor layer to improve device performance as taught by Mizuta (FIG. 7; Col. 1).

8. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martinez et al. (US PGPub 2003/0235974) and Mizuta et al. (US Patent 6,483,135 of record) as applied to claim 15 above, and further in view of Sheppard et al. (US Patent 2001/0017370 of record).

Regarding claim 16, as described above, Martinez and Mizuta substantially read on the invention as claimed, except Martinez and Mizuta do not teach a contact layer formed by an undoped AlGaIn. Sheppard teaches an undoped AlGaIn contact layer (17) to improve the characteristics of the device [0011, 0026]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Martinez and Mizuta to make the contact layer out of undoped AlGaIn to improve the characteristics of the device as taught by Sheppard [0011, 0026].

Claim 17: Mizuta teaches the field plate portion extends to an upper portion of said contact layer (FIG. 7).

9. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martinez et al. (US PGPub 2003/0235974) in view of Hirokawa (US PGPub 2002/0043697 of record).

Claim 19: Martinez teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer and an electron supply layer, a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode, and said insulating film is a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film elements (FIG. 8; [0030, 0034-0048]).

Martinez does not teach a size of said field plate is not lower than $0.3\mu\text{m}$. Hirokawa teaches a size of said field plate is not lower than $0.3\mu\text{m}$ to improve device performance (Abs, [0026]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have specified the field plate length

of Martinez to be not lower than .3 μm to improve device performance as taught by Hirokawa (Abs, [0026]).

Claim 20: Hirokawa teaches a size of said field plate is not lower than 0.5 μm .

Claim 21: Hirokawa teaches a size of said field plate portion is not more than 70% of a distance between said gate electrode and said drain electrode.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US PGPub 2001/0015446 of record) in view of Mizuta et al. (US Patent 6,483,135 of record).

Claim 12: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer and an electron supply layer, a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (FIG. 6E; [0061-0068]).

Inoue does not teach said drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween. Mizuta teaches said drain electrode side is lower than said gate electrode side in a

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dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween to improve device performance (FIG. 7; Col. 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Martinez to have drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer to improve device performance as taught by Mizuta (FIG. 7; Col. 1).

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US PGPub 2001/0015446 of record) in view of Mizuta et al. (US Patent 6,483,135 of record) as applied to claim 12 above, and further in view of Martinez et al. (US PGPub 2003/0235974)

Regarding claim 13, as described above, Inoue and Mizuta substantially read on the invention as claimed, Inoue teaches said insulating film being made of a compound containing silicon and nitrogen as constituent elements, said insulating film between said field plate portion and a surface of said semiconductor layer structure and Mizuta teaching the insulating film is a multilayered film, said gate electrode side is formed by a single layer film of the first insulating film and said drain electrode side is formed by the multilayered film including said first insulating film and said second insulting film in said insulating film between said field plate portion and a surface of said semiconductor layer structure.

Inoue and Mizuta do not teach said insulating film is a multilayered film including a first insulating film and second insulating film said first insulating film being made of a compound containing silicon and nitrogen as constituent elements and said second insulating film having a dielectric constant lower than that of the first insulating film. Martinez teaches said insulating film is a multilayered film including a first insulating film (71, 72) and second insulating film (73), said first insulating film being made of a compound containing silicon and nitrogen as constituent elements and said second insulating film having a dielectric constant lower than that of the first insulating film to improve device performance (FIG. 8; Col. 1-2). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the insulating film taught by Inoue and Mizuta to have the properties claimed above to improve device performance as taught by Martinez (FIG. 8; Col. 1-2).

Response to Arguments

12. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-F 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./
Examiner, Art Unit 2814

/Theresa T. Doan/
Primary Examiner, Art Unit 2814